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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,984	11/29/2001	Ludwig Leipold	WMP-SME396	4247

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EXAMINER
BENSON, WALTER

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/997,984	Leipoid et al.
Examiner	**Art Unit**
Walter Benson	2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov 29, 2001* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4, 6, and 9-15* is/are rejected.

7) ☒ Claim(s) *5, 7, 8, and 16-18* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 6
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Taruya (US Patent No. 5,584,275 and Taruya hereinafter).

4. As to claim 1, Taruya discloses an apparatus and method for generating a control signal after a predeterminable period of time, which comprises:

applying a voltage to an inductor at a beginning of a time measurement (col. 4, lines 17-19);

outputting, via a current threshold value detector, the control signal if a current through the inductor exceeds a predeterminable threshold value (col. 4, lines 32-37).

5. As to claim 6, Taruya discloses an apparatus and method for generating a control signal after a predeterminable period of time, which comprises:

which comprises using the inductor as an ignition coil of an ignition system of an internal combustion engine (col. 2, lines 13-17).

6. As to claim 9, Taruya discloses an apparatus and method for generating a control signal after a predeterminable period of time, which comprises:

forming the control signal as a switching signal (col. 2, lines 40-46).

7. As to claim 10, Taruya discloses a timing circuit for generating a control signal after a predeterminable period of time, comprising:

an electric circuit having a voltage source (2, Fig. 1);

a controllable switch connected to the voltage source (14, Fig 1);

an inductor connected to said controllable switch 11, Fig. 1);

a current threshold value detector with a control output connected to said inductor (42, Fig. 1; col. 4, lines 30-32).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-4, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taruya in view of Sandri et al. (US Patent No. 5, 745, 352 and Sandri hereinafter).

Although the apparatus and method disclosed by Taruya shows substantial features of the claim invention (discussed above), it fails to disclose:

a method which comprises flowing the current through a measuring resistor, and measuring a voltage drop across the measuring resistor using a voltage threshold value detector, the voltage drop serving as a measure of the current through the inductor [claims 2 and 11].

where the controllable switch is a field-effect transistor [claim 14].

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Taruya, as evidenced by Sandri.

In an analogous art, Sandri discloses a control loop of a converter inhibits current flow through an inductor as long as the current remains below a minimum threshold set value having:

a method which comprises flowing the current through a measuring resistor, and measuring a voltage drop across the measuring resistor using a voltage threshold value detector, the voltage drop serving as a measure of the current through the inductor [claims 2 and 11] (col. 3, lines 54-56).

where the controllable switch is a field-effect transistor [claim 14] (col. 3, lines 56-60). Given the teaching of Sandri, a person having ordinary skill in the art at the time the invention was made would have readily recognized the desirability and advantages of modifying Taruya by employing the well known or conventional features conversion and switching, such as disclosed by Sandri, in order to reduce circuit complexity and provide dedicated monitoring and switching circuits.

10. As to claim 3, Taruya discloses a timing circuit for generating a control signal after a predeterminable period of time, comprising:

measuring a current rise at the inductor, and logically combining the voltage drop and the current rise in a logic circuit, and the logic circuit generates the control signal (col. 5, lines 14-19).

11. As to claim 4, Taruya discloses a timing circuit for generating a control signal after a predeterminable period of time, comprising:

using one of the current threshold value detector, the voltage threshold value detector and the logic circuit to drive an electronic switch, the electronic switch switches off the current through the inductor (col. 5, lines 6-10).

12. As to claims 12 and 13, Taruya discloses a timing circuit for generating a control signal after a predeterminable period of time, comprising:

where the controllable switch has a control input (14, Fig. 1);

the inductor is a primary winding of an ignition coil of an electronic ignition system of an internal combustion engine 11, Fig. 1);

the control output [G, Fig. 1] of the current/voltage threshold value detector is connected to the control input of said controllable switch (col. 5, lines 1-6).

13. Claim 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taruya in view of Farrington et al. (US Patent No. 6,166,927 and Farrington hereinafter).

Although the apparatus and method disclosed by Taruya shows substantial features of the claim invention (discussed above), it fails to disclose:

where the field-effect transistor is an insulated gate bipolar transistor.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Taruya, as evidenced by Farrington.

In an analogous art, Farrington discloses a converter for converting an input voltage to a selectable output voltage having:

where the field-effect transistor is an insulated gate bipolar transistor (S1, Fig. 2; col. 3, lines 27-33).

Given the teaching of Farrington, a person having ordinary skill in the art at the time the invention was made would have readily recognized the desirability and advantages of modifying Taruya by employing the well known or conventional features conversion and switching, such as disclosed by Farrington, in order to reduce circuit complexity and provide dedicated monitoring and switching circuits in which the source and drain operate as short-circuit when a voltage exceeding the threshold voltage is applied across the gate and drain.

Allowable Subject Matter

14. Claims 5, 7-8, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach or suggest individually or in combination an apparatus and method which includes measuring the current rise at the inductor and a voltage drop across the electronic switch. Then logically combining the current rise and the voltage drop across the electronic switch with one another in the logic circuit. The logic circuit outputs the control signal. Further the prior art fails to suggest or teach a

timing circuit where the voltage source has a first pole and a. second pole. The current threshold value detector has a further voltage threshold value detector with a first input, a second input, a third input and an output. The current threshold value detector has a logic circuit with a first input, a second input, a first output and a second output. The primary winding of the ignition coil has a first terminal connected to the first pole and to said first input of the further voltage threshold detector, a second terminal connected to the second input of the further voltage threshold value detector and to the collector terminal of the field-effect transistor. The first emitter of said field-effect transistor connected through the measuring resistor to the gate electrode of the field-effect transistor, to the first output of the logic circuit, to the third input of the further voltage threshold value detector and to the second pole of the voltage source; the measuring resistor has a first terminal connected to the first input of the voltage threshold value detector; the voltage threshold value detector has an output connected to said first input of the logic circuit. The output of the further voltage threshold value detector connected to the second input of the logic circuit. The second output of the logic circuit connected to the gate electrode of the field-effect transistor.

Prior Art Made of Record

15. A. Yamada et al. (US Patent No. 6,505,605 B2) discloses a control system an internal combustion engine;

B. Roederer (US Patent No. 5,548,471) discloses a DC-powered spark-generating circuit for igniting fuel;

C. Tozzi (US Patent No. 6,006,156) discloses an apparatus for diagnosing and controlling an ignition system which includes an ignition coil controllable by an ignition control circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (703) 306-4525. The examiner can normally be reached on Monday to Thursday and alternate Fridays from 6:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached on (703) 308-0750. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9318); Before-Final or (703) 872-9319; After-Final.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

Walter Benson WB
Patent Examiner
April 30, 2003

N. Le
Supervisory Patent Examiner
Technology Center 2800